Boost Switching Power Supply

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1. Introduction

There exist two types of DC-DC converters: linear and switched. Linear power supplies tend to have a simpler circuit configuration when compared to switching regulators. Linear power converters are limited to stepping down an input voltage and tend to be larger in physical size. Linear power supplies are also less efficient than switching power supplies. Switched power supplies are smaller, more efficient, and are capable of both stepping up and stepping down a voltage. The boost converter is a switching power supply that steps up a DC input voltage and supplies a regulated, higher, DC output voltage to a load. This report will focus on the theory, design, layout, and simulation of a practical boost converter circuit. Figure 1 is a simplified diagram of the boost converter circuit. The circuit has two states, one where the switch is open, and another when it is closed. Let us consider the closed switch case first. The right half of the circuit can be ignored since the diode will not be forward biased. With the switch closed, we are applying a constant voltage to an inductor. This will cause the current through the inductor to increase linearly with a slope of V_{in} / L. As the current through the inductor increases, the inductor absorbs and stores the supplied energy from the voltage source in the form of a growing magnetic field. This process continues until the switch is opened. Now we analyze the circuit with the switch opened, assuming the switch had been closed for some period of time beforehand. The inductor has now built up a current which needs to flow somewhere. This current (I_{out}) flows through the diode and charges the capacitor to a voltage V_{out} and delivers power to the load while the switch is open. Suppose we change the state of the switch periodically. Calculations show that the output voltage depends on the input voltage and the percent of time the switch is closed. In practice, the switch is an N-channel MOSFET (NMOS). The NMOS gate is controlled by a PWM control circuit. The control circuit uses feedback from the output to make the decision of closing or opening the switch. This control circuit was our design.

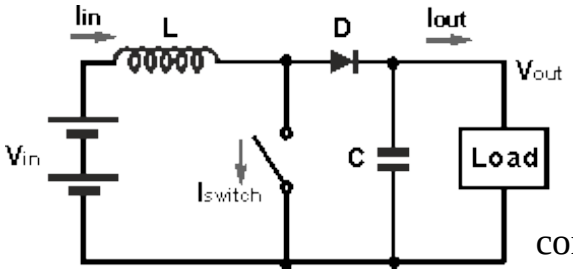
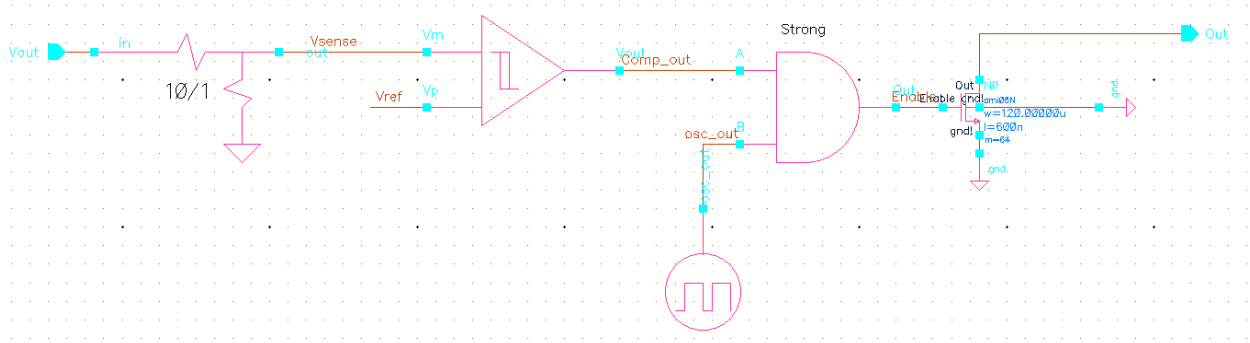


Figure 1: Boost switching power supply

2. Design

Control Loop

The control loop is the circuitry that opens and closes the NMOS. In reality, the control loop and NMOS switch are contained in an IC package. The control loop allows us to regulate the output voltage. The circuit uses the voltage at the load, V_{out}, as an input and compares it with a steady reference voltage (which is a fraction of the desired voltage). After comparing the two analog voltages, the circuit will decide whether to allow our oscillating signal to the gate of the NMOS.



Referring to the figure, we see that V_{out} is attenuated by a 10/1 resistive voltage divider before being compared to V_{ref}, the output of the bandgap. If V_{out} is lower than the reference voltage, then Enable will be logic high. The NAND gate and inverting buffer can be viewed as an AND gate. With that perspective, we can reduce the analysis to say that we are simply **gating the clock**. If V_{out} is greater than our reference voltage, the switch will remain off, allowing the inductor to supply its energy to the load. This is the behavior we want.

There are many design choices to be made. For example, how should we size the switch? How large should the driving buffer be? What should be the frequency of our oscillator? These questions affect the design and require information about the external circuit. The next section of the report will explore the details of each component and its operation.

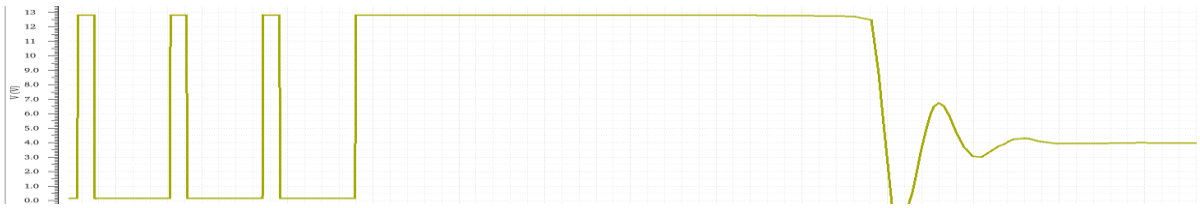


Figure 3:Voltage at the drain of the NMOS switch

Bandgap

The bandgap is a circuit designed to output a constant reference voltage ideally independent of temperature and supply voltage. For this design, an output voltage of 12.5 V was specified, and earlier in the course, we laid out a bandgap that produced a reference voltage of 1.25 V, hence the 10/1 voltage divider.

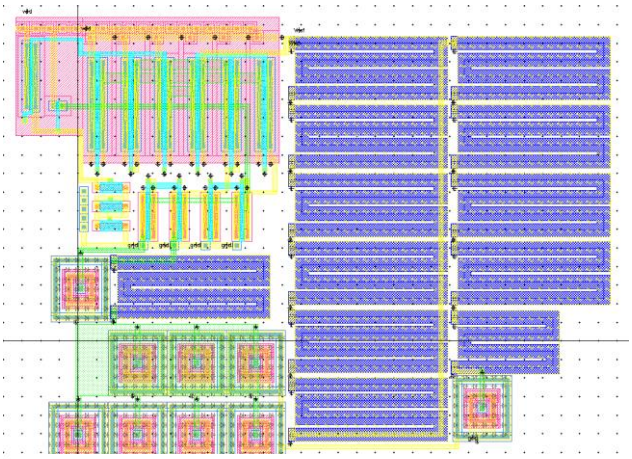


Figure 4: Bandgap layout

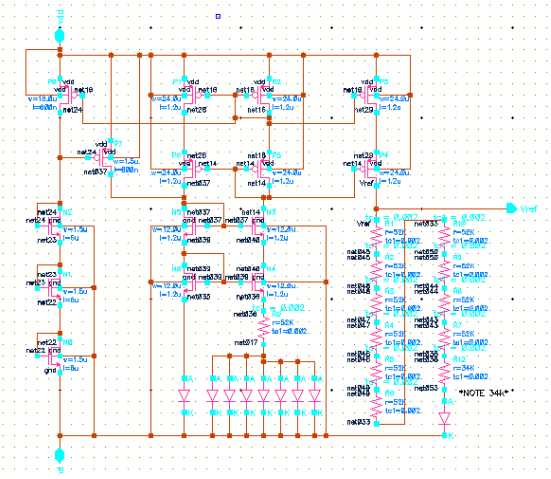


Figure 5: Bandgap schematic

There are two behaviors we are interested in with the bandgap. We would like to see how the circuit performs with a changing supply voltage, and how the circuit performs in different temperature conditions. The following curves illustrate these two behaviors. On the left we observe the output voltage while sweeping the input voltage through the range given in the project specifications. On the right we see the output voltage through a temperature range of 0 C to 100 C while keeping the supply voltage at 5 V.

When sweeping the supply voltage, the output only changes by 3 mV. The output is more sensitive to temperature though, dropping by 8 mV as temperature increases.

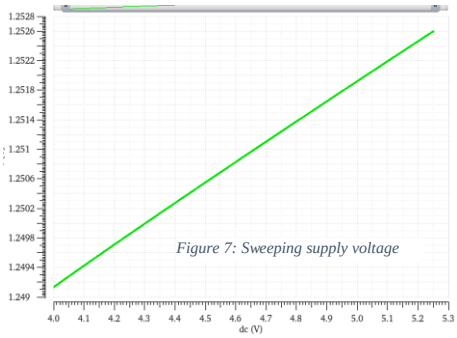


Figure 7: Sweeping supply voltage

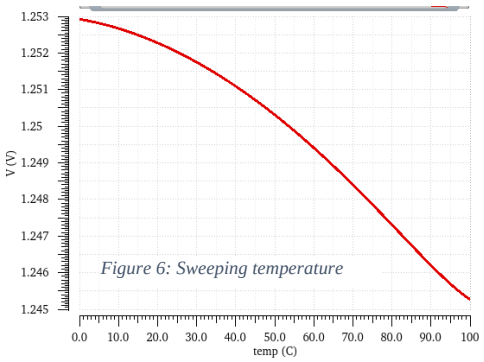
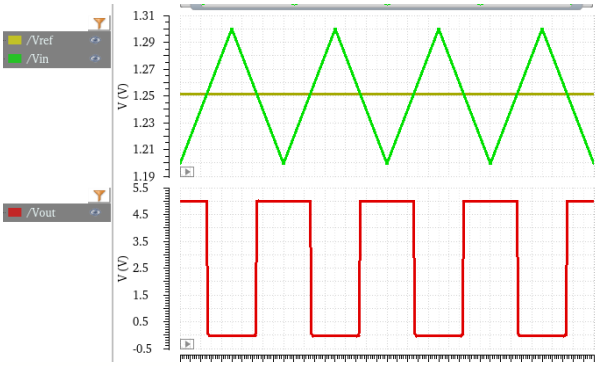


Figure 6: Sweeping temperature

These characteristics should be sufficient for our design.

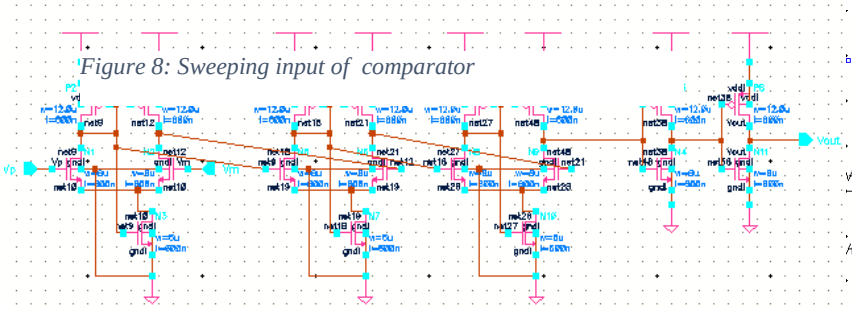
Comparator

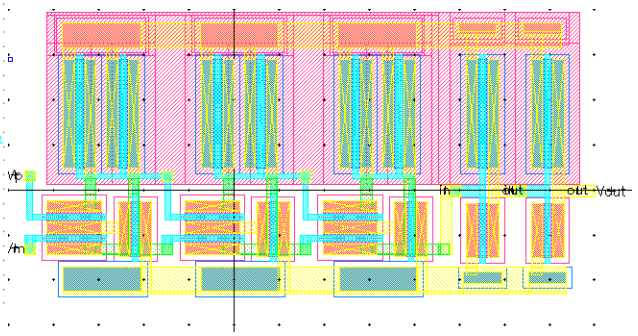
The comparator is essential to the decision making process. In operating this circuit, one input will be held constant by the bandgap, the other input will be the output of our converter. If the output voltage is greater than our reference, then the comparator outputs a logic 0, otherwise it will output a logic 1. An important behavior of the comparator is how sensitive is it to differences in the input. Ideally, we want a comparator that responds to the smallest difference in voltage, this is impractical because noise would cause such a comparator to oscillate when the inputs are very close in voltage. Thus, we would like a certain hysteresis of the comparator. That is, an upper and lower value where the comparator will switch values. We want this to be as small as possible while avoiding false switching. I achieved this behavior by using 3 stages of differential amplifiers, sent through fast inverters at the output to square the signal. The 3 stages will produce the sensitivity we are looking for without being too susceptible to noise.



In this image, Vout is the enable signal for our NAND gate. We can see the output is a decisive switch right when the input crosses Vref.

Figure 8: Sweeping input of comparator





Oscillator

The ring oscillator is the constantly running clock that we will be gating based on the output of the previous stage. When designing the clock, we want a fast switching frequency so we can keep the inductor value and the ripple voltage small. However, the clock cannot be too fast since we need to drive the switch which will have a large input capacitance. Also, since we will be adjusting the duty cycle such that when the circuit is enabled, the switch is mostly closed, and we want to give the inductor a chance to supply current to the load before closing the switch again. Through trial and error, I landed on an oscillator that conserved area but was also slow enough for our purposes. This oscillator has a frequency of 2.34 MHz with a duty cycle of around 80%. The duty cycle was adjusted by using inverters that were not identical in each stage. For example, the first inverter in a pair is of size 24u/6u, and the next inverter is of size 6u/24u, both with lengths of 6u. Since the t_{PHL} will be slower for each stage because of the bigger PMOS inverters, the oscillator switches high and stays there longer because of the extra time it takes for the inverter to fully output a 1. A fast inverter was used at the output to square off the signal and maintain inversion, since the original signal will not have decisive switching points.

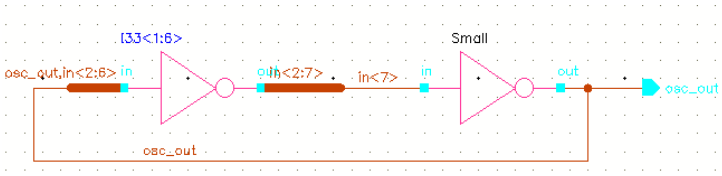


Figure 9: Oscillator schematic

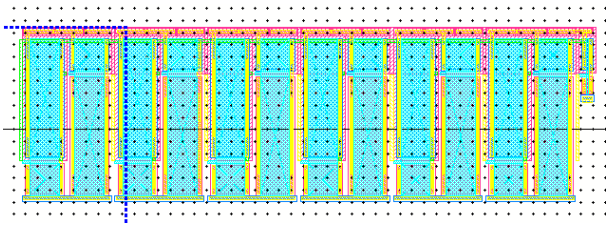


Figure 10: Oscillator layout

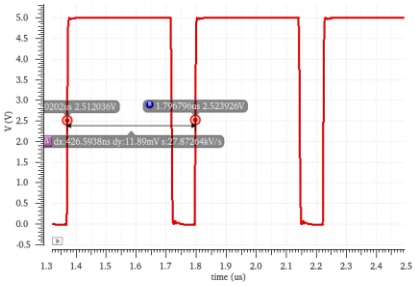


Figure 11: Oscillator output waveform

I tried different duty cycles at the same frequency. When the duty cycle was around 60%, it made the circuit more efficient but the circuit did not perform well at lower supply voltages. A higher duty cycle during the switching phase causes the inductor to source more current, but this extra current is needed at a lower input voltage.

Strong AND Gate

This gate is what will allow the oscillator signal to drive the NMOS switch. Since the NMOS is large, the input capacitance will be significant and will require a strong driver. Our approach in this design is using a small NAND gate, then a strong inverting buffer to build a strong AND gate used to drive the NMOS.

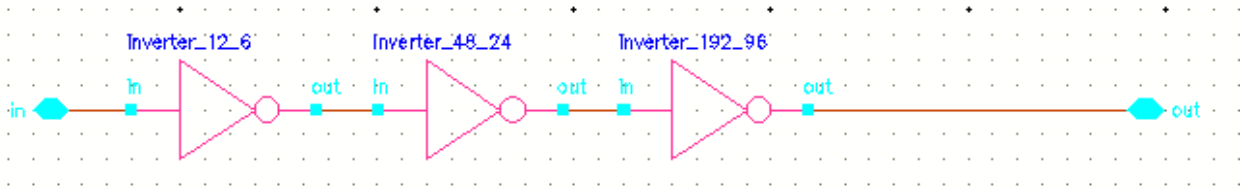
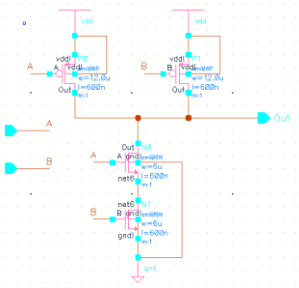


Figure 12: Inverting buffer used to drive large NMOS



This circuit gates our clock. When it is enabled, the drain of our NMOS oscillates between Vout and ground. When the circuit is disabled, the switch is steadily open since it's off, and no current flows in the inductor since the switch is open and the diode is reverse biased. This property is what makes this converter efficient.

Figure 13: NAND gate schematic

NMOS Switch

This part of our IC is what interfaces with the external circuit. When sizing the switch, we have to consider both the input capacitance and the on resistance. The switch should be sharply driven by our control loop, this is the purpose of the buffer that drives the switch. Second, the switch should have a low enough resistance such that it can drain all of the current from the inductor, forcing the drain terminal to ground. This improves efficiency and reduces the startup time. To increase current flow, we want our W/L ratio to be as high as possible. I achieved this by making a 7680u/0.6u NMOS using 120u/0.6u FETs with a multiplier of 64.

Figure 14: Power NMOS

Inductor

Selecting the inductor requires information about the switching frequency, the duty cycle, and the average inductor current.

$$L = \frac{Vout * D * (1 - D)}{f * \Delta i_L}$$

All of the relevant information can be obtained from the control loop, plugging in the values, I chose an inductance of 75u H, a standard inductor value. Choosing an inductor that is too small can result in lower efficiency because it will draw more current from the source, and the NMOS must be able to handle more current. An inductance that is too large will be costly, but can store more energy in each cycle. We want an inductor/NMOS combination such that the drain of the NMOS goes to ground quickly, and the magnitude of the current is minimized. The inductance I chose results in acceptable efficiency at the range of input voltages given.

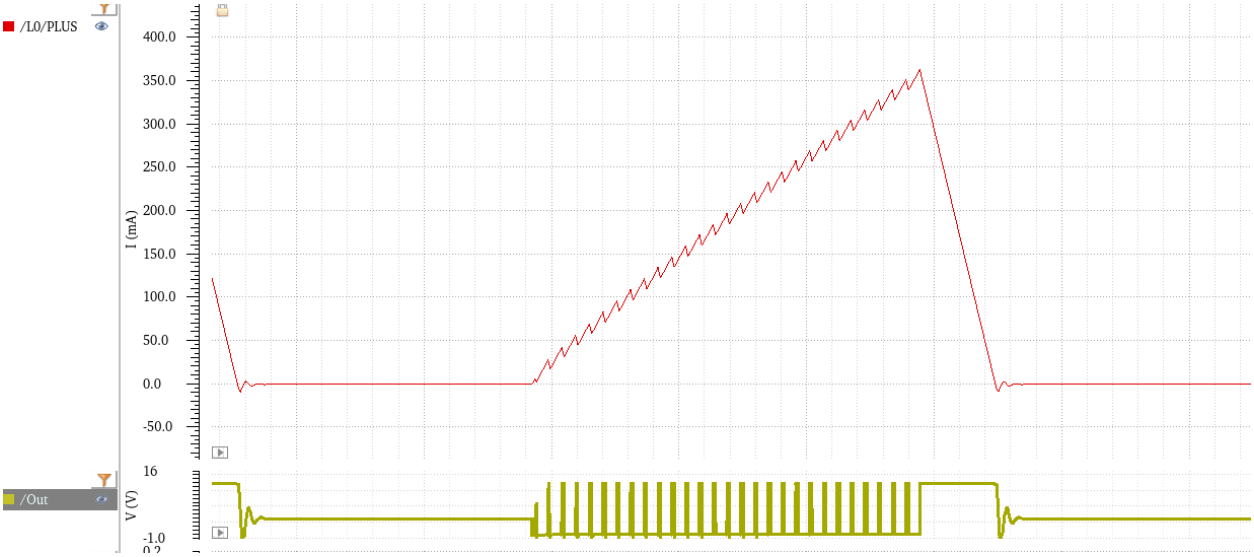


Figure 15: Inductor current and drain voltage

3. Layout

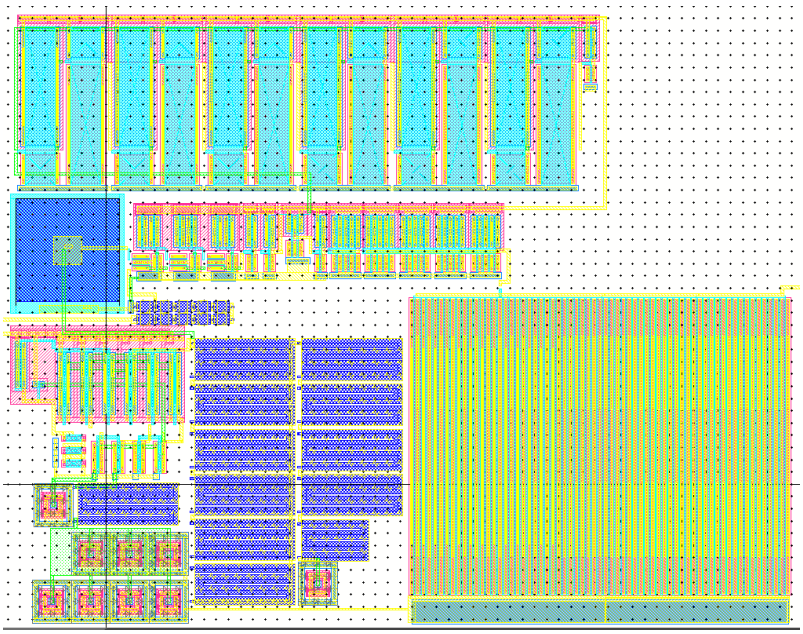


Figure 16: Layout view

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The net-lists match.

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        rewired                   0         0
        size errors               0         0
        pruned                    0         0
        active                  202       103
        total                   202       103

                                  nets
        un-matched                0         0
        merged                    0         0
        pruned                    0         0
        active                   68        68
        total                    68        68

                              terminals
        un-matched                0         0
        matched but
        different type            0         0
        total                     5         5
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Figure 17: LVS check

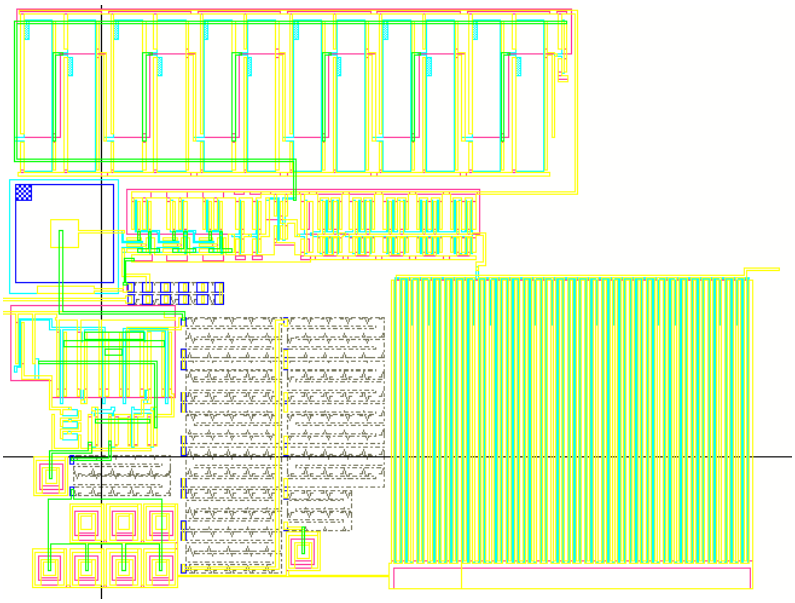

Figure 18: Extracted view

In drafting the layout, the approach was structural and hierarchical. I made sure every component passed checks before connecting them together. The layout has three terminals, VDD and Vout inputs are on the left, and the output voltage (drain of NMOS) is on the right side of the layout.

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*********   Summary of rule violations for cell "CG_proj_f21 layout"   *********
   Total errors found: 0
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Figure 19: DRC check

4. Simulation

Output and efficiency

My design is able to supply up to 62 mA through the whole input voltage range. The efficiency is best with a heavier load, which makes sense. The output voltage can deviate, on average, from the nominal voltage by up to 70 mV. This is not optimal and can be improved. Efficiency ranges between ~75-85%. Again, this is not ideal as some boost converters can have efficiencies of up to 95%, but those converters could have a tighter constraint on the input supply voltage and likely supply less current. Our design is a practical circuit that can reliably supply high currents.

Load (Ω)

VDD (V)	200	300	400	500	600
4.00	12.51	12.49	12.49	12.49	12.49
4.25	12.52	12.51	12.51	12.50	12.50
4.50	12.55	12.53	12.52	12.51	12.51
4.75	12.56	12.54	12.52	12.53	12.52
5.00	12.57	12.54	12.54	12.53	12.53
5.25	12.57	12.56	12.53	12.53	12.53

Average Vout

Note: $I_{Load} =$ Vout/Load

$$\eta = \frac{Vout * I_{load}}{VDD * avg(I(VDD))}$$

Load (Ω)

VDD (V)	200	300	400	500	600
4.00	86.0%	84.4%	83.8%	81.6%	79.9%
4.25	85.9%	86.2%	83.8%	81.3%	80.6%
4.50	86.8%	85.7%	81.9%	79.9%	78.8%
4.75	86.8%	85.7%	82.7%	84.8%	78.0%
5.00	86.0%	82.3%	80.4%	77.7%	76.2%
5.25	86.1%	83.0%	82.7%	77.3%	75.9%

Efficiency

Temperature

To test the temperature dependence, I kept the load at 500 Ohms and the input voltage at 4.25 V.

Temperature (°C)	Average Vout
0	12.52
20	12.51
40	12.50
60	12.48
80	12.46
100	12.43

The circuit starts to output a lower voltage as temperature increases. This is due to the bandgap's output dropping with temperature. Since our output depends on the reference provided by the bandgap, we would expect our output to drop with temperature accordingly.

Ripple

Using the best performing parameters, (4.25 V input, 500 Ohm load), the ripple voltage has an amplitude of 35 mV. With the worst performing parameters, (5.25 V, 200 Ohm load), the ripple voltage has an amplitude of 200 mV. Depending on the use case, this may or may not be acceptable.

Figure 20: Ripple voltage

The ripple voltage can be improved by using a larger filter capacitor at the output, but this would cost more. I kept the capacitor at a small 10 uF. As with the rest of the design, there were choices to make after looking at the tradeoffs.

5. Conclusion

The boost converter I designed is not perfect. Commercial boost converters have efficiencies of up to 95%. My converter was less efficient. It could have been improved by having a slower frequency, but this would result in higher ripple and a larger device. Our design was only expected to supply 20 mA to a load but my design was able to supply up to 62 mA reliably. I was proud of this accomplishment. One other flaw with the design is that the high frequency will produce electromagnetic interference. This issue can be fixed with proper filtering circuitry. The project was thorough and extremely practical. I went from the conceptual understanding of a circuit to having a real working model laid out in silicon. The project applied all of the course material in a natural and comprehensive way.