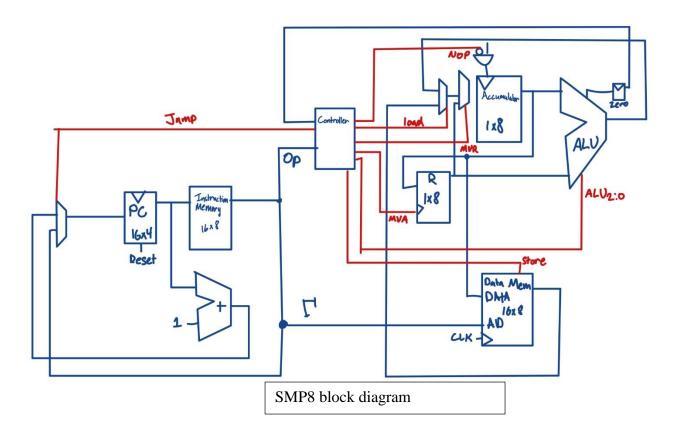
UNIVERSITY O	F NEV	ADA LAS VEGAS. DEPARTMENT O	F ELECTRICAL AND C	OMPUTER ENGIN	EERING LABORATORIES.
Class:	Cpl	E300L	Semester:	Spring 2021	
Points		Document author:	es		
		Author's email:	Georgc4@unl	v.nevada.edu	J
		Document topic:	Final Project		
Instructor's	s com	nments:			

1. Introduction / Theory of Operation

This report will detail the design and operation of the SMP8, a very simple 8-bit microprocessor designed with similar principles as the MIPS single-cycle processor. The processor consists of a combinational control unit with a small datapath. The datapath includes several multiplexers, instruction and data caches, 2 general registers, an ALU and other supporting components. The processor supports 16 instructions including a NOP instruction. The processor is not very powerful but it was designed for simplicity and not efficiency. We wrote testbenches for 2 test codes and implemented them on the DE2 FPGA board as well as in simulation (VCS).

2. Results of Experiments



¥	Instruction	NOP	LOAD	STORE	MVA	MVR	JUMP	ALU
		8	8 7	6	5	4	3	2:0
	1 NOP	1	0	0	0	0	0	100
2	2 LDAC	0	1	0	0	0	0	100
:	3 STAC	1	0	1	0	0	0	100
4	4 MVAC	0	0	0	1	0	0	100
:	5 MOVR	0	0	0	0	1	0	100
(6 JUMP	1	0	0	0	0	1	000
1	7 JMPZ	1	0	0	0	0	Z	000
8	B JPNZ	1	0	0	0	0	!Z	000
9	ADD	0	0	0	0	0	0	000
1(SUB	0	0	0	0	0	0	001
1'	1 INAC	0	0	0	0	0	0	010
12	2 CLAC	0	0	0	0	0	0	011
1:	3 AND	0	0	0	0	0	0	100
14	4 OR	0	0	0	0	0	0	101
1:	5 XOR	0	0	0	0	0	0	110
10		0	0	0	0	0	0	111

BØ 10 A0 A0 74 30 Machine code for test 1 (left) and 50 F0 test 2 (right) A0 E0 30 6A 80 24 22 00 00 00

Design Codes:

```
module smp8 (input clk, reset,
output [3:0] pc,
input [7:0] instr,
output [7:0] AC);
wire zero, nop, load, store, mva, mvr, jump;
wire [2:0] alucontrol;
controller c(instr[7:4], zero, nop, load, store, mva, mvr, jump, alucontrol);
datapath dp(clk, reset, nop, load, store, mva, mvr, jump, alucontrol, zero, pc, instr, AC);
endmodule
```

Top module

```
module controller (input [3:0] op,
input zero.
output nop,
output load, store,
output mva, mvr,
output jump,
output [2:0] alucontrol);
reg [8:0] controls
    ign { nop, load, store, mva, mvr, jump, alucontrol } = controls;
 case(op)
     4'h0: controls = 9'b100000100; //NOP
     4'h1: controls = 9'b010000100; //LDAC
    4 h1: controls = 9 b010000100; //LDAC
4'h2: controls = 9'b101000100; //STAC
4'h3: controls = 9'b000100100; //MVAC
4'h4: controls = 9'b00001000; //MVAC
4'h5: controls = 9'b100001100; //JUMP
4'h6: controls = zero ? 9'b100001100 : 9'b100000100; //JMPZ
4'h7: controls = (~zero) ? 9'b100001100 : 9'b100000100; //JPNZ
                                                                                             Control unit
     4'h8: controls = 9'b00000000; //ADD
     4'h9: controls = 9'b00000001; //SUB
     4'hA: controls = 9'b00000010; //INAC
     4'hB: controls = 9'b00000011; //CLAC
4'hC: controls = 9'b00000010; //AND
4'hD: controls = 9'b00000101; //OR
4'hE: controls = 9'b00000110; //XOR
     4'hF: controls = 9'b000000111; //NOT
endmodule
module datapath (input clk, reset,
input nop,
input load, store,
input mva, mvr,
input jump,
input [2:0] alucontrol,
output zero,
output [3:0] pc,
input [7:0] instr,
output [7:0] AC);
wire AC_clk;
wire [7:0] aluout;
                                                                           Datapath stitched together
 assign AC_clk = ~nop & clk;
wire [3:0] pcnext, pcplus1;
wire [7:0] acnext, ldout, R, datamem;
wire zeronext;
flopr #(4) pcreg(clk, reset, pcnext, pc);
adder pcadd1 (pc, 4'h1, pcplus1);
mux2 #(4) pcmux(pcplus1, instr[3:0], jump, pcnext);
// register file logic
flopr #(8) AC_reg(AC_clk, reset, acnext, AC);
flopr #(8) R_reg (mva, reset, AC, R);
mux2 #(8) ldmux(aluout, datamem, load, ldout);
mux2 #(8) mvmux(ldout, R, mvr, acnext);
dmem dmem (clk, instr[3:0], store, AC,datamem);
alu alu(AC, R, alucontrol, aluout, zeronext);
flopr #(1) zeroreg(clk, reset, zeronext, zero);
endmodule
```



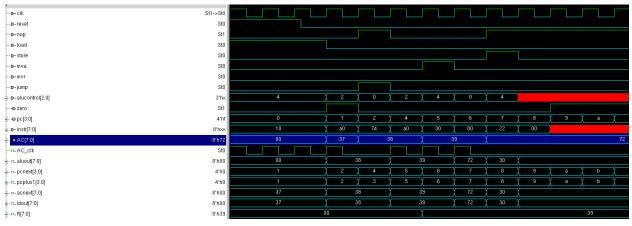
```
module alu (a,b,sel, out, zero);
input [7:0] a,b;
input [2:0] sel;
output reg [7:0] out;
output reg zero;
  out = 0;
  zero =1'b0;
    always @ (*)
begin
case(sel)
    3'b000:
       out=a + b;
    zero = (out ==0);
end
    3'b001:
    zero = (out ==0);
end
      out= a - b;
     3'b010:
    out= a + 1;
zero = (out ==0);
end
     3'b011:
    begin
out= 0;
    zero = 1;
end
     3'b100:
    begin
out= a & b;
        zero = (out ==0);
     3'b101:
      out= a | b;
       zero = (out ==0);
    3'b110:
       out=a ^ b;
        zero = (out ==0);
    3'b111:
       out= ~a;
    zero = (out ==0);
end
    default: begin
out = 8'h00;
            zero = 1'b1;
endmodule
```

ALU

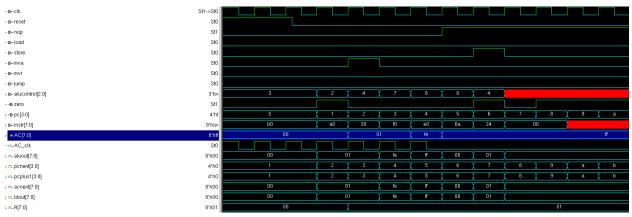
```
`include "top.v"
module testbench();
reg clk;
reg reset;
wire [3:0] pc;
wire [7:0] AC, instr;
// instantiate device to be tested
top dut (clk, reset);
// initialize test
initial
begin
reset <= 0; # 22; reset <= 1;
end
// generate clock to sequence test:
always
begin
clk <= 1;
    # 5;
    clk <= 0;
    # 5; // clock duration
end
// check results
always @ (negedge clk)
begin
if (dut.pc == 15) begin
$display("Simulation completed");
$stop;
end
end
endmodule</pre>
```

Testbench, values were verified in waveform

Waveforms:



Accumulator ends at 0x72 = 114 = 55 + 1 + 1 + (57) CORRECT!



Accumulator ends at $0xFF = 255 = \sim (0+1) \wedge 1$ CORRECT!

Test Code 1 Video Demo

Test Code 2 Video Demo

Timing:

mmand Info Su	immary of P	aths																			
Slack		From Nod			To Node		Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay										
			pr:AC_reg		8:smp8 datapath:dp flopr		dk	dk	1.000	-3.520	4.765										
			pr:AC_reg		B:smp8 datapath:dp flopr		dk dk	dk dk	1.000	-3.520	4.763 4.735										
			pr:AC_reg pr:AC_reg		8:smp8 datapath:dp flopr 8:smp8 datapath:dp flopr		dk	dk	1.000	-3.520	4.728										
	smp8 data	path:dp[fi	pr:AC_reg	a[5] smp	8:smp8 datapath:dp flopr		dk	dk	1.000	-3.517	4.693										
			pr:AC_reg		8:smp8 datapath:dp flopr		dk	dk	1.000	-3.517	4.689										
			pr:AC_reg		8:smp8 datapath:dp flopr	:zeroreg[q[0]	dk	dk	1.000	-3.520	4.658										
-7.174 smp8:	smo8ldata	oath:dolfi	or:AC_real	of 21 smp	8:smp8ldatapath:dplflopr	:zerorea la la 101	dk	dk	1.000	-3.520	4.652										
h #1: Setup slack	k is -7.287	(VIOLAT	ED)							Path #1: 5	etup slack is -	-7.287 (VIOLA	'ED)								
th Summary Sta	atistics	Data Path	Wavefi	rm Extr	a Fitter Information					Path Summ	ary Statistic	ics Data Pati	Waveform	Extra P	itter Inforn	nation					
ta Arrival Path																					
Total	Incr	RF	Type	Fanout	Location		Element			^											
0.000	0.000					launch edge tir	ne			-2.248 ns											
✓ 7.401	7.401					clock path				Launch C1	ock Launch										
0.000	0.000					source latency				Council of	~~								J L		ון
0.000	0.000			1	PIN_M23	dk				Setup Rel	tionship	1.0 ns									
0.000	0.000	RR	IC	1	IOIBUF_X115_Y40_N8	dk~input i				Secup Rel	acconsnip —										
0.650	0.650	RR	CELL	6	IOIBUF_X115_Y40_N8	dk~input o					. ⊢	Latch									
3.387	2.737	RR	IC	1	LCCOMB_X74_Y1_N6	smp8 dp AC_c				Latch Clo	*										
5.277	1.473	RR	IC	1	LCCOMB_X74_Y1_N6 CLKCTRL_G17	smp8 dp AC_c	ik/compout ik~dkctrl/indk[0]													_	—
5.277	0.000	RR	CELL	8	CLKCTRL_G17		ik~akctrijnakjuj ik~akctrijoutak			Data Arri	/al										
6.803	1.526	RR	IC	1	FF_X73_Y2_N5	smp8 dp AC_r								7,404							
7.401	0.598	RR	CEL	1	FF 173 12 N5		tanath-dnifloor-AC	reala[0]		Clock Del	19			7.401 n			>				
ta Required Path																					
Total	Incr	RF	Type	Fanout	Location		Element			Data Dela	a d								4.765		
1.000	1.000					latch edge time	-														
¥ 4.881	3.881					dock path				Slack								-7.287 n	8		
1.000	0.000					source latency															
1.000	0.000			1	PIN_M23	ck				Data Regu					Y						
1.000	0.000	RR	IC	1	IOIBUF_X115_Y40_N8	dk∾inputli															
1.000	0.070	00	(C)			dk-input)				Data kegu	irred -				^						
	0.000										ired				^						
Slack					To Node		Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela	37			^						
Slæck		From Nod	e .		Traini de Unite d'An Ain		Launch Clock dk	Latch Clock dk	Relationship 8.500		+	9y			^						
Słack 0.213 smp8:	smp8 dataj	From Nod path:dp/file		q[0] smp	To Node	r:zeroreg q[0]			(Constanting)	Clock Skew	Data Dela	5 y			^						
Slack 0.213 smp8: 0.243 smp8:	smp8 data smp8 data	From Nod path:dp]fili path:dp]fili path:dp]fili path:dp]fili	e ppr:AC_reg pr:AC_reg	q(0) smp q(0) smp q(2) smp	To Node 8:smp8(datapath:dp)flop 8:smp8(datapath:dp)flop 8:smp8(datapath:dp)flop	r:zeroregiq(0) r:zeroregiq(0) r:zeroregiq(0)	dk dk dk	dk dk dk	8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520	Data Dela: 4.765 4.763 4.735	зу			^						
Slack 0.213 smp8: 0.243 smp8: 0.243 smp8: 0.250 smp8:	smp8 data smp8 data smp8 data	From Nod path:dp]fil path:dp]fil path:dp]fil path:dp]fil	e pr:AC_reg pr:AC_reg pr:AC_reg	q(0) smp q(0) smp q(2) smp q(0) smp	To Node 8:smp8(datapath:dp)flop 8:smp8(datapath:dp)flop 8:smp8(datapath:dp)flop 8:smp8(datapath:dp)flop	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	dk dk dk dk	dk dk dk dk	8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520 -3.520	Data Dela 4.765 4.763 4.735 4.735	89			^						
Slack	smp8 data smp8 data smp8 data smp8 data smp8 data	From Nod path:dp[flip path:dp]flip path:dp]flip path:dp]flip path:dp]flip path:dp]flip	e ppr:AC_regi ppr:AC_regi ppr:AC_regi ppr:AC_regi	q[0] smp q[0] smp q[2] smp q[0] smp q[5] smp	To Node 8:smp8(datapath:d) (fing 8:smp8(datapath:d) (fing 8:smp8(datapath:d) (fing 8:smp8(datapath:d) (fing 8:smp8(datapath:d) (fing	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	dk dk dk dk dk dk	dk dk dk dk dk dk dk	8.500 8.500 8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520 -3.520 -3.517	Data Dela 4.765 4.763 4.735 4.728 4.693	8y			^						
Slack smp8: 0.213 smp8: 0.243 smp8: 0.250 smp8: 0.288 smp8: 0.288 smp8:	smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data	From Nod path:dp [fi path:dp]fi path:dp]fi path:dp]fi path:dp]fi path:dp]fi path:dp]fi	e ppr:AC_regi ppr:AC_regi ppr:AC_regi ppr:AC_regi ppr:AC_regi	q(0) smp q(0) smp q(2) smp q(0) smp q(0) smp q(5) smp q(5) smp	To hode 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	ck ck ck ck ck ck ck	dk dk dk dk dk dk dk dk	8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520 -3.520 -3.517 -3.517 -3.517	Data Delar 4.765 4.763 4.735 4.735 4.735 4.693	зу			^						
Slack 0.213 smp8: 0.213 smp8: 0.243 smp8: 0.288 smp8: 0.288 smp8: 0.292 smp8: 0.292 smp8:	smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data	From Nod path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili	e ppr:AC_regj ppr:AC_regj ppr:AC_regj ppr:AC_regj ppr:AC_regj	q[0] smp q[0] smp q[2] smp q[2] smp q[5] smp q[5] smp q[2] smp	To Node Sumpi jatapathud ji figa Sumpi jatapathud ji figa	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	ck ck ck ck ck ck ck ck ck	dk dk dk dk dk dk dk dk dk	8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520 -3.517 -3.517 -3.517 -3.520	Data Dela 4.765 4.763 4.735 4.735 4.693 4.693 4.658	3y			^						
Slack 0.213 smp8: 0.215 smp8: 0.250 smp8: 0.250 smp8: 0.288 smp8: 0.292 smp8: 0.320 smp8: 0.320 smp8: 0.320 smp8:	smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data	From Nod path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili path:dp/fili	e ppr:AC_regi ppr:AC_regi ppr:AC_regi ppr:AC_regi ppr:AC_regi	q[0] smp q[0] smp q[2] smp q[2] smp q[5] smp q[5] smp q[2] smp	To hode 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog 8:smp8 (datapath:d) flog	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	ck ck ck ck ck ck ck	dk dk dk dk dk dk dk dk	8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.527 -3.517 -3.517 -3.517 -3.517 -3.517 -3.520	Data Delar 4.765 4.763 4.773 4.728 4.693 4.689 4.659 4.652				^						
Slack 0.213 smp8: 0.213 smp8: 0.243 smp8: 0.288 smp8: 0.328 smp8: 0.320 smp8: 0.320 smp8: 0.326 smp8: 0.326 smp8: 0.326 smp8:	smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data smp8 data	From Nod path:dp]fil path:dp]fil path:dp]fil path:dp]fil path:dp]fil path:dp]fil path:dp]fil path:dp]fil	e pr:AC_regi pr:AC_regi pr:AC_regi pr:AC_regi pr:AC_regi pr:AC_regi pr:AC_regi	q[0] smp q[0] smp q[2] smp q[0] smp q[5] smp q[5] smp q[2] smp q[2] smp	To hide Sampi (datapathd) (hig Sampi (datapathd) (hig	r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0] r:zeroreg q[0]	ck ck ck ck ck ck ck ck ck	dk dk dk dk dk dk dk dk dk	8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500 8.500	Clock Skew -3.520 -3.520 -3.520 -3.520 -3.517 -3.517 -3.517 -3.517 -3.517 -3.520 Path #1:	Data Delar 4.765 4.763 4.773 4.723 4.693 4.693 4.659 4.659 4.659 5 Setup slack is	is 0.213			^						
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Timing was fixed by changing clock to have **8.5 ns period**. Both test code 1 and 2 contain 9 instructions, each taking a single cycle, so 8.5 ns * 0 = 76.5 ns execution time

3. Conclusions & Summary

In conclusion, this project was an appropriate culmination of our studies of computer architecture. We were tasked with building an 8-bit processor in Verilog by first designing a block diagram that supports all the instructions specified, then implementing it in code and testing its operation on an FPGA development board and in simulation with waveforms. After putting a good effort into the block diagram, the code was the easy part. No changes were made to the block diagram after the drawing was finalized, meaning it worked exactly as designed which is something I am proud of. The project as a whole is worthy to go on my resume and I look forward to increasing my knowledge of computer architecture and possibly pursue a career in it.